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POWER STORAGE IN D OCEAN

D4.1. Design Report of the EESS which includes SC Cell selection, DC/DC power components selection & others.

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1. OVERVIEW

This document describes OCEM proposal for the design of the Electric Energy Storage System EESS for the POSEIDON project.

The EESS will be part of a power electronics system used to feed a load; the system will be mainly composed by a bidirectional DC/DC converter connected to a DC line (minimum voltage 750V, maximum voltage 850V) and a supercapacitors storage bank.

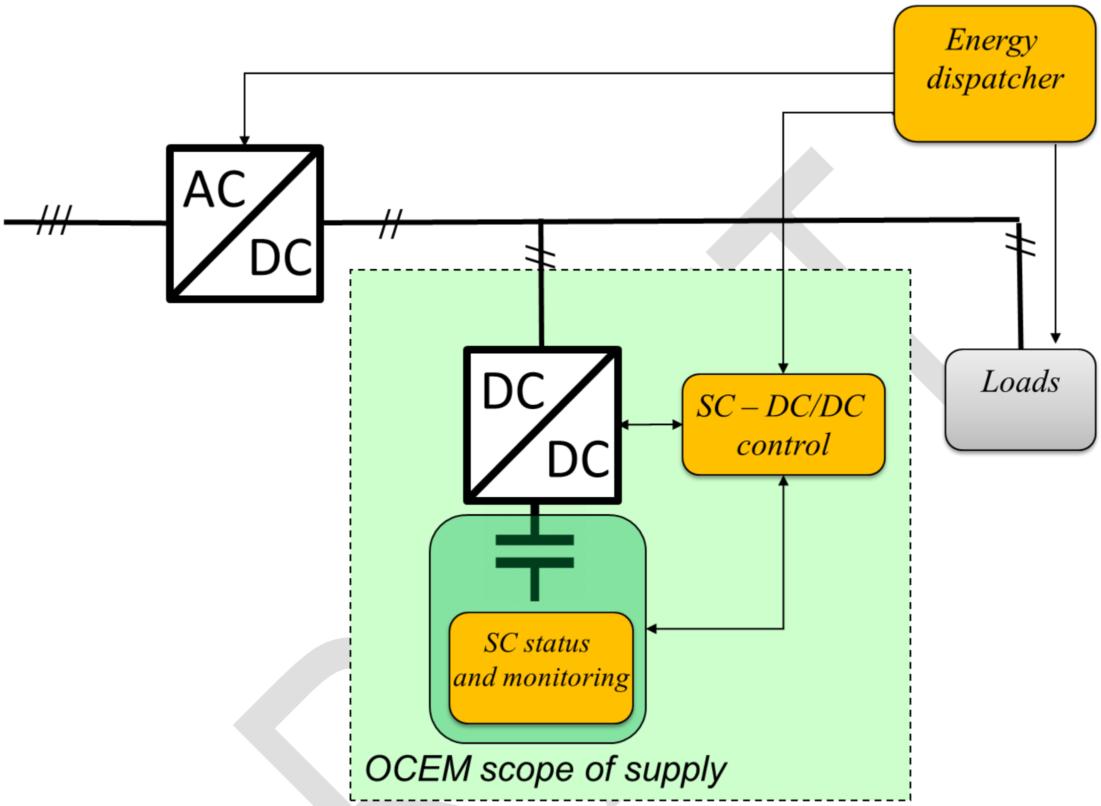


Figure 1 Block diagram of the system

The DC/DC converter will initially charge the SC bank before operation up to a fixed charging voltage, maximum 750V; during the operation the SC bank will be discharges/charged following the power or current reference delivered by the main control system, indicated as "Energy Dispatcher". The controller assures that during the operations, the SC voltage remains constrained between minimum (≥ 300 V) and maximum (≤ 750 V) voltage. This voltage excursion allows to exchange a net energy of 84 % of the total energy stored in the SC bank.

The SC bank must not be discharged completely during operation, because the more the voltage drops, the more the current through the DC/DC converter increases, for this reason is not convenient to discharge a supercapacitor bank below its 40%.

The complete discharge of the SC bank is done only at the end of the operations, where a resistor bank is connected to the supercapacitor through a normally closed contactor. The resistor is sized to dissipate all the SC energy. It assures an exponential decay of the SC voltage, so that the approach of zero voltage is slowly achieved. This will protect individual SC cells, that are connected in series, from voltage inversion that could happen if the SC voltage is abruptly brought to zero.

The control system included in the scope of supply of OCEM take care of controlling the current delivered to the common DC-bus as well as to perform diagnostic and protection of both the DC/DC converter and SC bank.

The DC/DC converter topology is derived by a ready-made and proven design of the so called TGPS Power Module that is already used in several OCEM applications. One significative installation is at TRIUMF, for the main cyclotron magnet, rated 20 kA 80 A. In Figure 3~~Figure 3~~ the main PS of the TRIUMF cyclotron is reported. In Figure 2~~Figure 2~~ the 3D model of the power module and the IGBT modules on which the module is based of it is reported.

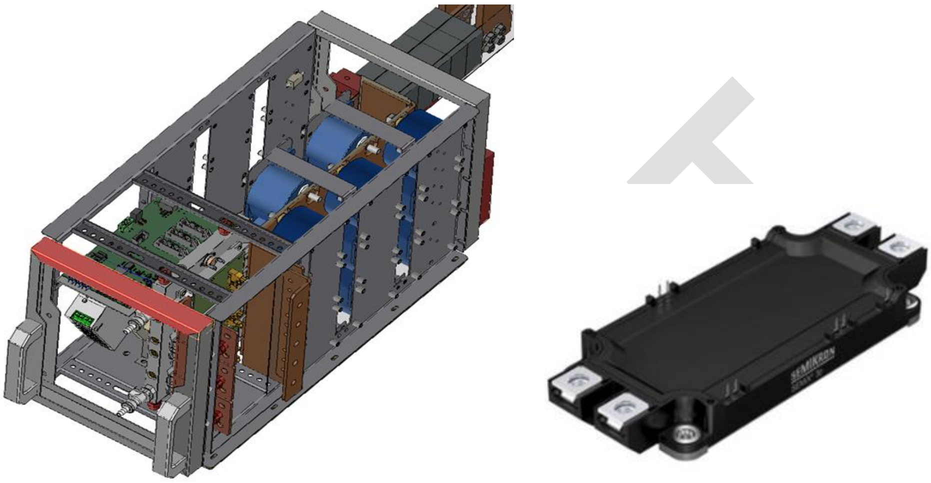


Figure 2 Power module structure and adopted IGBT module format

Figure 3 Example of a complete Power Supply (the picture is related to the TRIUMF Main Cyclotron)

The SC bank will be made up by several SC modules, connected in series and parallels in order to achieve the desired requirements in terms of peak voltage and stored energy. Each module has is composed by several cells and will have an integrated interface through which is possible monitoring the status of each module.

OCEM already has experience in designing supercapacitors bank, in Figure 4~~Figure 4~~ it is shown the supercapacitors bank made for a superconductive magnet power supply already delivered to a customer on Fusion Energy Experiment.

Figure 4 Supercapacitor bank made for Tokamak Energy

1.1. REQUIREMENTS

In Table 1~~Table 1~~, the main requirements, on which of the EESS sizing has been done, are summarized.

Table 1 Main specifications

Characteristics	**Unit**	**Value**
Maximum LES voltage at the start of the discharge (charge voltage)	[V]	750
Minimum LES voltage during the discharge	[V]	> 300
Total LES capacitance END OF LIFE	[F]	12.7
LES discharge energy (from 800 V to 500 V)	[MJ]	> 3
Typical discharge duration	[s]	30
Maximum duty cycle (discharge/recharge)	[s/s]	30/300
Maximum peak current	[A]	< 400
Installation	-	Marine
Expected lifetime	[years]	20

2. SIMULATION REPORT

The simulation model and simulation results shown hereafter in this section are aimed to show the behaviour of the proposed configuration. The simulation activity was carried out in a first moment with the software tool PLECS (https://www.plexim.com/products), this first phase was useful in order to size the components and making thermal considerations.

In a second moment, an equivalent electrical model was built on OpenModelica an open-source Modelica-based modelling and simulation environment.

In this chapter, the main outcomes of the simulation activity will be presented.

2.1. PLECS MODEL

In Figure 6~~Figure 4~~ the general scheme of the model built on PLECS is shown.

The DC line has been simulated through an ideal DC source at 850V, then there is the DC/DC converter, that is made of three IGBT half-bridge modules in parallel connection.

Then, between the converter and the SC bank, there is a LC filter with damping branch, exploiting the fact that the filter branch has time constant much lower than the one of the supercap branch, the HF content of the current ripple coming from the DC/DC converter is filtered and does not flow into the supercap branch. Without the filter, the current ripple would generate significative losses and heating, due to the high values of ESR that typically a supercap bank has.

The filter has been designed with a cut-off frequency of 50 Hz, in such way the ripple component due to the switching frequency (5kHz) gets an attenuation of -80 dB (the Butterworth filter has an attenuation of -40 dB per order of magnitude).

On the right, the diagram of the amplitude attenuation of Butterworth filters of different orders:

In red the 1st order,

in blue the 2nd order (our case),

in green the 3rd order.

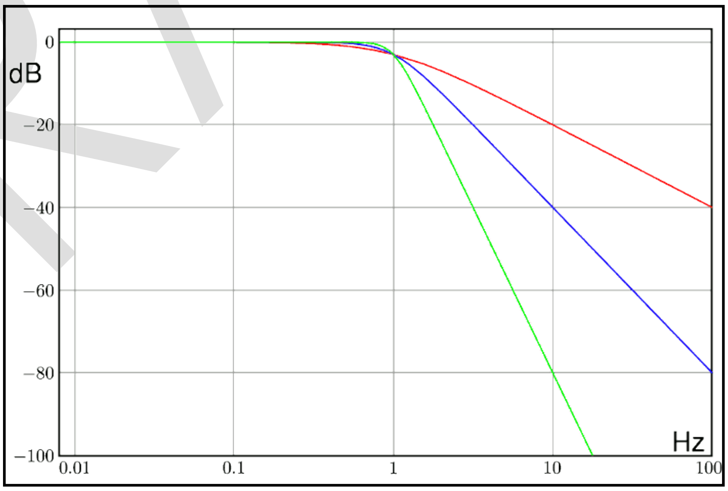


Figure 5 Butterworth filter attenuation

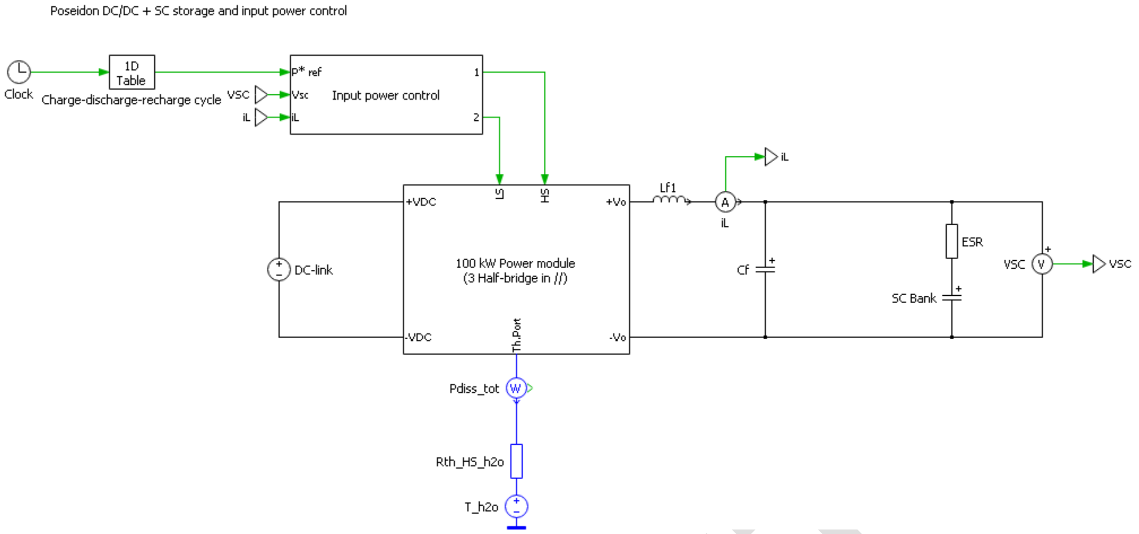


Figure 6 General model built on PLECS

The converter is realised through the parallel connection of three half bridge module. The top switches are controlled through the same driving signal, and the bottom switches through another one.

For this simulation, it has been considered that the bank has to deliver around 3MJ (2.5MJ requested + a margin of 0.5MJ for the possible losses) with a peak power of 120kW (100kW requested + a margin of 20kW for the possible losses).

Then the capacitance needed has been evaluated as:

$$E = \frac{1}{2}\, C\, (V_{initial}^2 - V_{final}^2)$$

$$C = \frac{2\, E}{(V_{initial}^2 - V_{final}^2)}$$

$$C = \frac{2\,(3\,MJ)}{(750^2 - 300^2)} = \mathbf{12,7\ F}$$

In Figure 7~~Figure 5~~ the inside of the DC/DC Converter block is depicted; the blue squares in figure represents the heatsinks of the IGBT modules, since also thermal simulations have been conducted, to be sure that the overheating in commutation devices are not an issue.

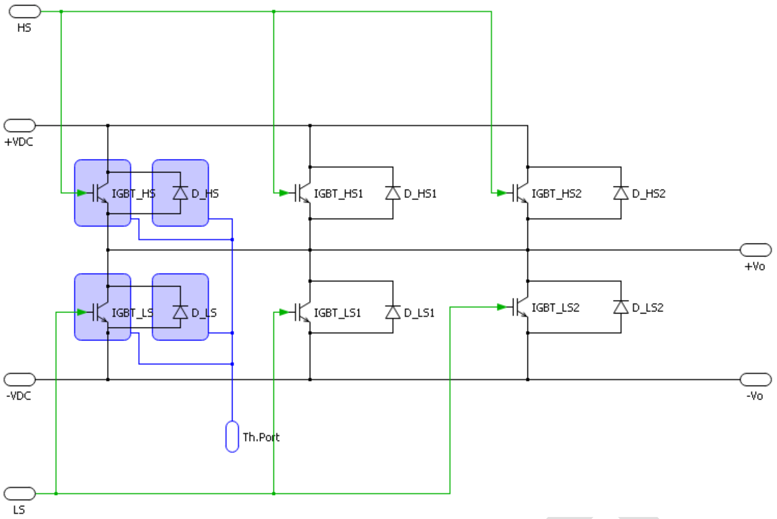


Figure 7 DC/DC converter

The control implemented (scheme in Figure 8~~Figure 6~~) takes in input a Power profile reference (Figure 9~~Figure 7~~), the SC voltage measurement and the total current measured on the DC/DC converter. Through the Power reference and the SC voltage measured, the current converter reference is generated, then it is compared to the measured converter current, and the error is regulated through a PI regulator, the output of the regulator, scaled, is used as modulating signal for the PWM block with switching frequency of 5kHz, that will generate the proper driving signals for the converter's IGBTs.

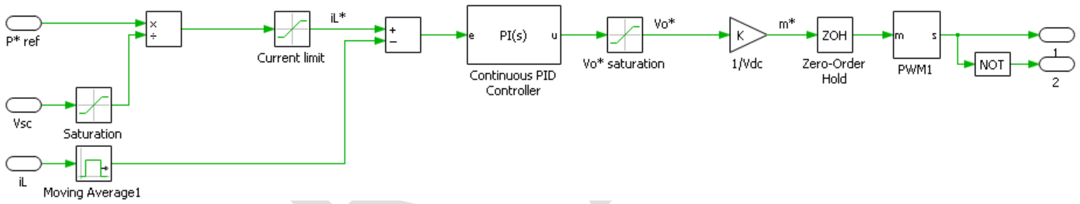


Figure 8 Control logic

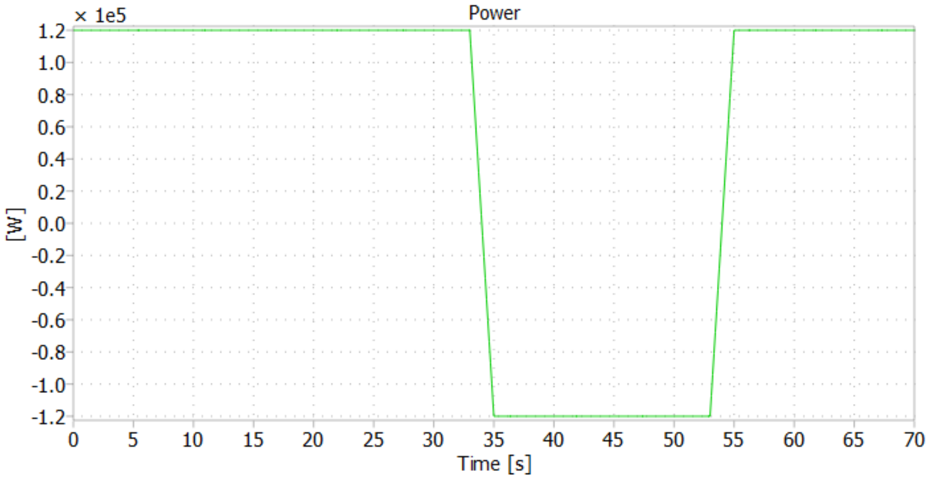


Figure 9 Power reference

2.1.1. OUTCOMES

In this subchapter there will be presented the main outcomes of the simulation work.

The case considered was the worst from the thermal point of view, i.e. the one in which the system has to work constantly at the peak power (120kW).

Figure 10~~Figure 8~~ shows the total current flowing through the converter (top plot), the DC line voltage (middle plot, green curve), the voltage across the SC bank (middle plot green curve) and the active power flowing through the system.

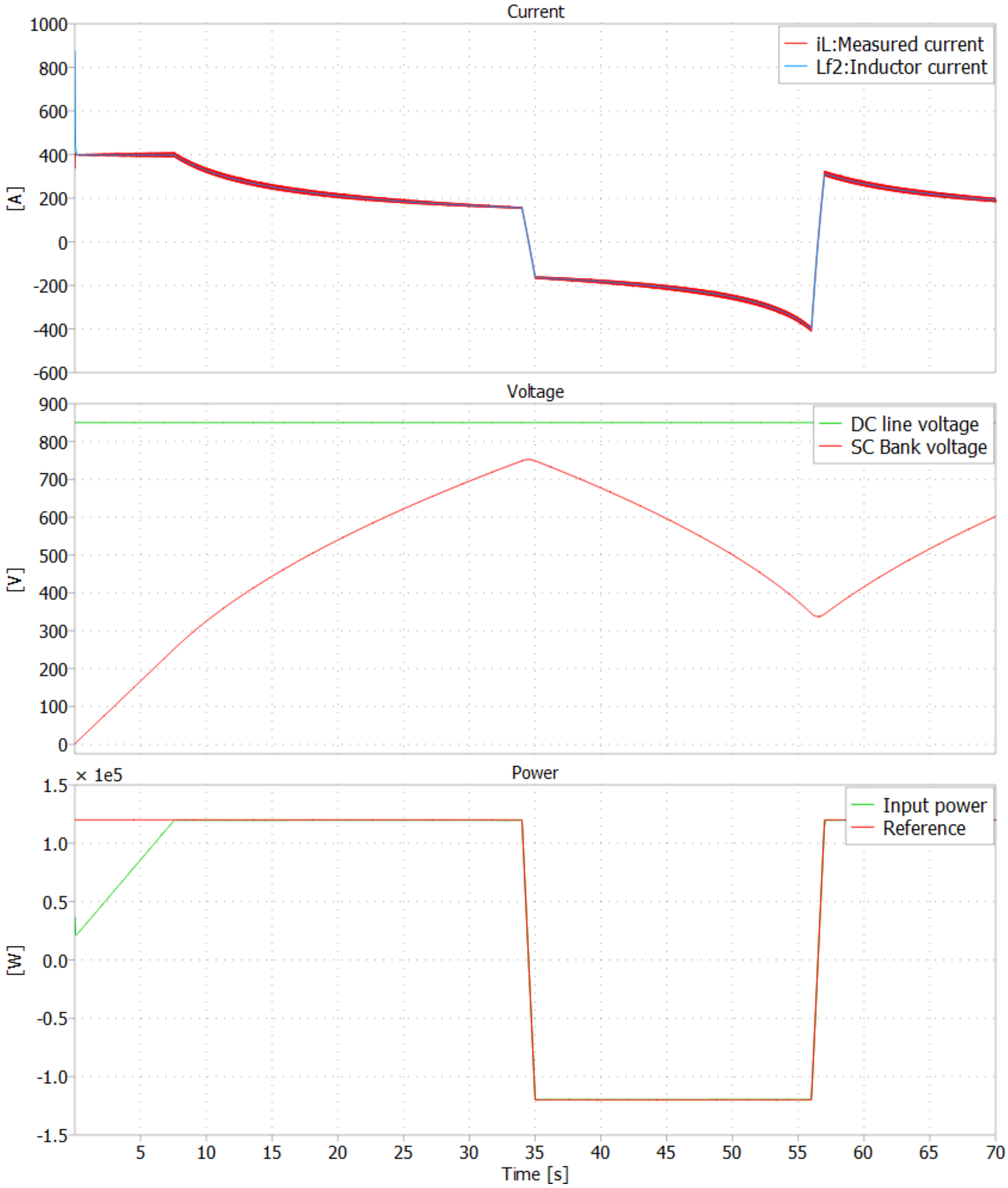


Figure 10 Outcomes plot

The SC bank releases the energy achieving a voltage drop from 750V to 370V, the measured power follows the reference with good precision.

To perform the thermal simulations, the thermal model of MITSHUBISHI CM600DX-34T has been considered, since this (or an equivalent component) will be implemented for this application. The profile of the estimated losses (both conduction and switching) and junction temperatures are reported in Figure 11~~Figure 9~~.

The highest stress corresponds to the initial condition in which the Supercap Bank has to be charged starting from 0V. This condition is verified only at the very beginning of the operation, since the bank will never be discharged below its 40% in operating conditions.

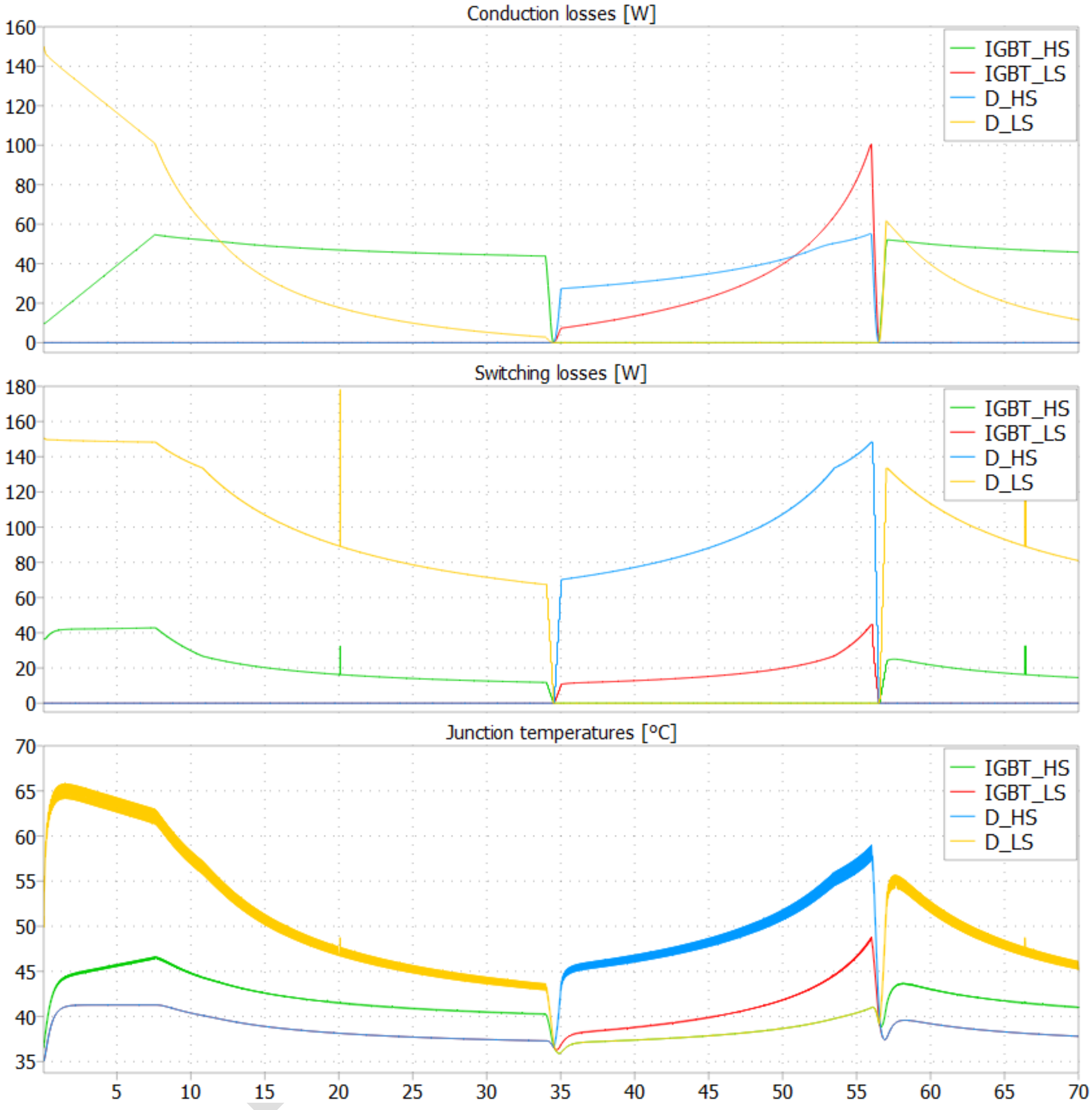


Figure 11 – Losses and temperatures

Anyway, the temperature level is safe in every operating point, this confirms that the power module water-cooled will handle the required currents without having heating issues.

2.2. OPENMODELICA MODEL

As anticipated before in this chapter, a second model on modelica has been built; this is a model based on average values, and it is intended to be integrated into the general model of the system made by the team of TPH S.L. The results obtained are comparable to the ones measured on the PLECS model; in Figure 12~~Figure 10~~ it is shown the OpenModelica model scheme.

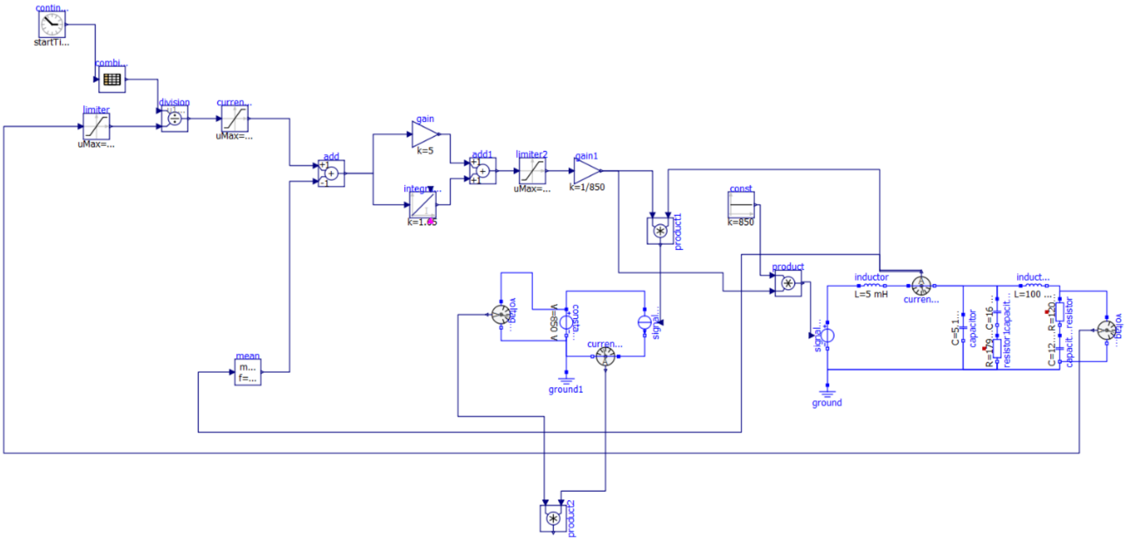


Figure 12 OpenModelica scheme

As outcome it is shown only the voltage profile of the Supercapacitor bank state of charge (Figure 13~~Figure 11~~), just to prove that the model is coherent to the accurate one built on PLECS.

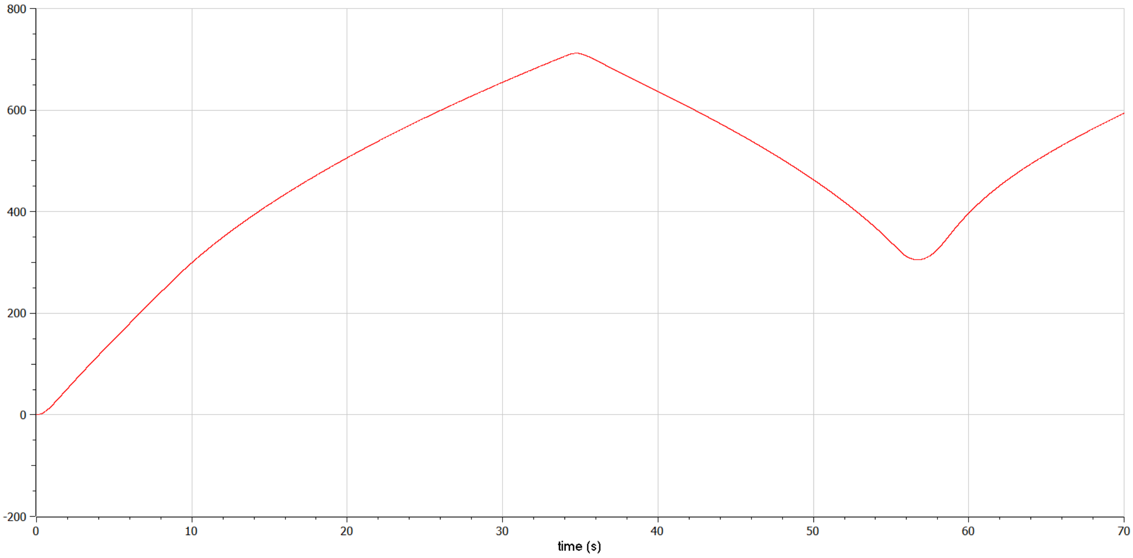


Figure 13 SC Bank voltage

3. COMPONENTS SELECTION

3.1. POWER MODULE

The individual power module (shown in Figure 14~~Figure 12~~) is a water-cooled unit provided with IGBTs in the standard 150 x 62 x 17 mm package and completed with IGBT drivers, diagnostic board, bus-bar and local DC-bus film capacitors.

The use of film capacitors also gives a strong contribution to the overall reliability of each module. Moreover, in case the module is used as a spare part and it is stocked for several years, it does not lose its electrical property during the stockage period.

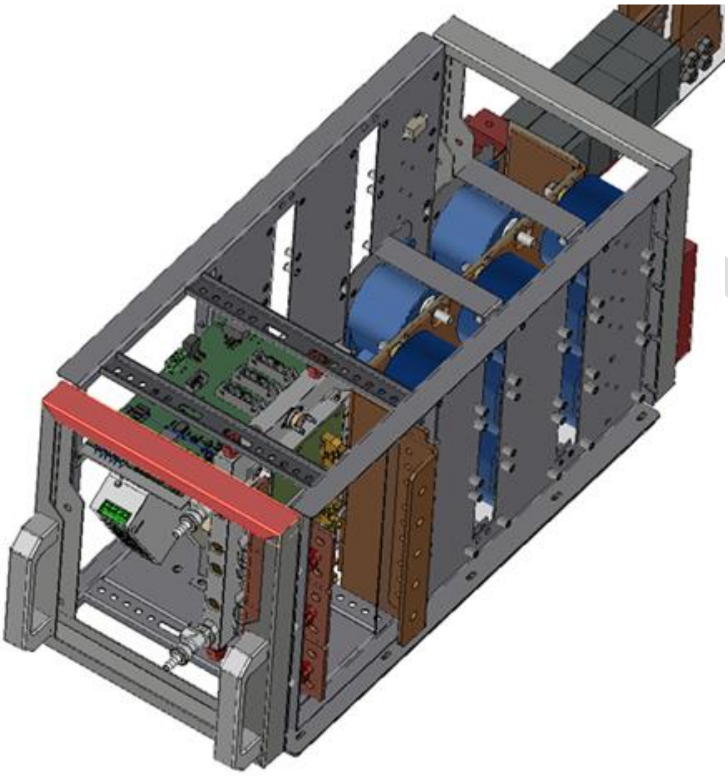


Figure 14 TGPS power module

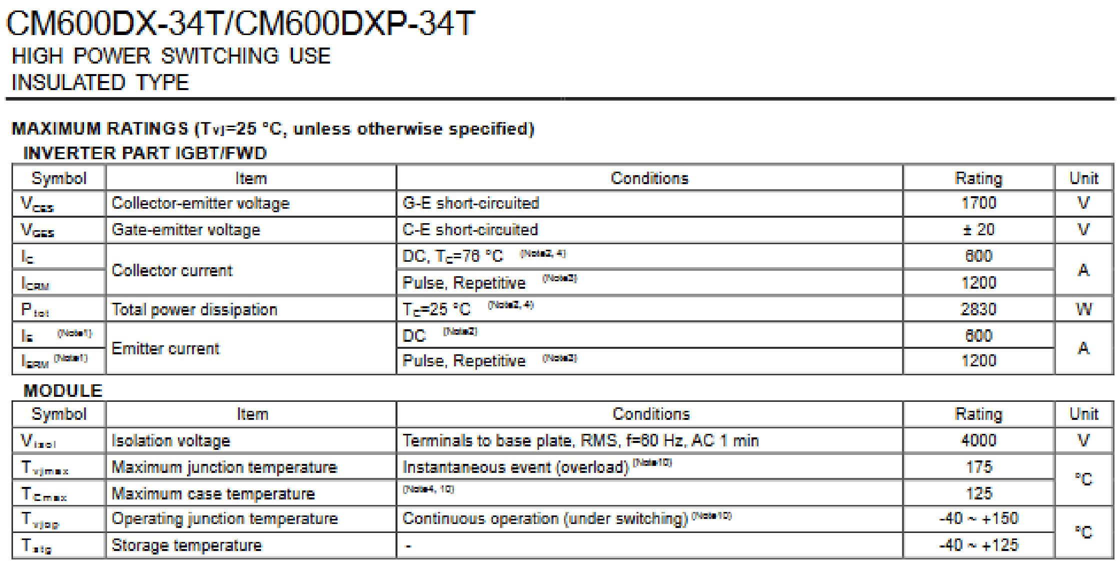
The cooling plate of IGBT is realized with only copper and stainless steel in contact with water. The capacitors are sized to withstand the ripple current of the IGBT. The power module can be configured to realize different converter topologies and can be equipped with different IGBT and capacitors voltage ratings. For the application presented in this document, the module is configured as Half-bridge with three 1700V IGBTs modules in parallel.

The connection between capacitors and semiconductors is made of low inductance laminated busbars.

The IGBT drivers used are delivered from power integrations and directly soldered to the IGBT.

IGBT switching signals and status feedback signals are provided through optic fibre for improved disturbance immunity.

In particular, the IGBT modules that will be implemented are the *MITSUBISHI CM600DX-34T* (



CM600DX-34T/CM600DXP-34T
HIGH POWER SWITCHING USE
INSULATED TYPE

MAXIMUM RATINGS (T_{vj}=25 °C, unless otherwise specified)
INVERTER PART IGBT/FWD

Symbol	Item	Conditions	Rating	Unit
V_{CES}	Collector-emitter voltage	G-E short-circuited	1700	V
V_{GES}	Gate-emitter voltage	C-E short-circuited	± 20	V
I_C	Collector current	DC, T_C=76 °C (Note2, 4)	600	A
I_{CRM}		Pulse, Repetitive (Note3)	1200	
P_{tot}	Total power dissipation	T_C=25 °C (Note2, 4)	2830	W
I_E (Note1)	Emitter current	DC (Note2)	600	A
I_{ERM} (Note1)		Pulse, Repetitive (Note3)	1200	

MODULE

Symbol	Item	Conditions	Rating	Unit
V_{isol}	Isolation voltage	Terminals to base plate, RMS, f=60 Hz, AC 1 min	4000	V
T_{vjmax}	Maximum junction temperature	Instantaneous event (overload) (Note10)	175	°C
T_{Cmax}	Maximum case temperature	(Note4, 10)	125	
T_{vjop}	Operating junction temperature	Continuous operation (under switching) (Note10)	-40 ~ +150	°C
T_{stg}	Storage temperature	-	-40 ~ +125	

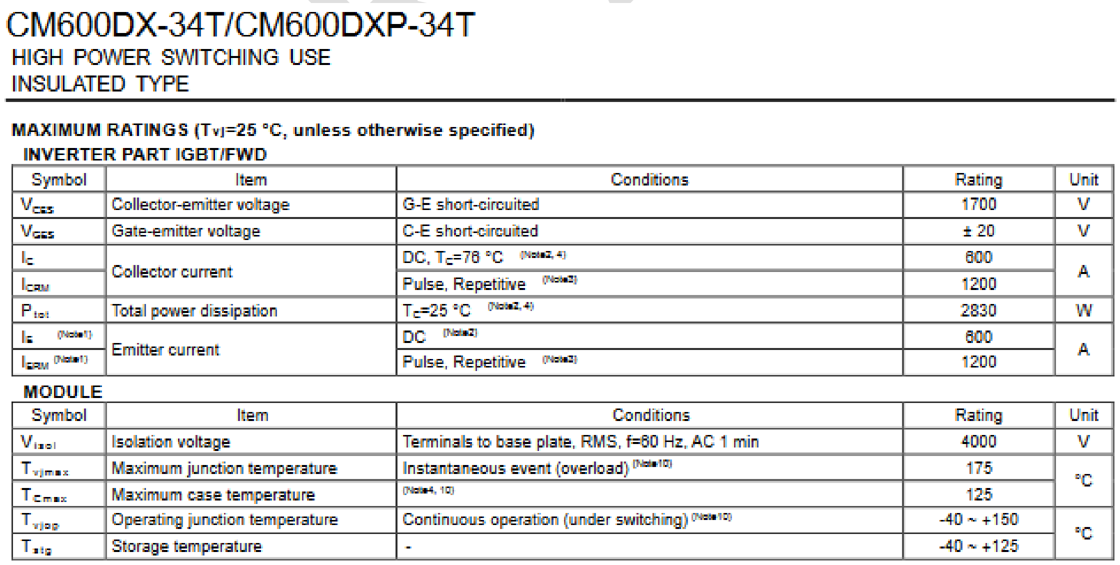
Figure 15~~Figure 13~~) or another equivalent IGBT module.

MITSUBISHI CM600DX-34T

DX

Collector current I_C .... 600 A
Collector-emitter voltage V_{CES} .... 1700 V
Maximum junction temperature T_{vjmax} .... 175 °C

- Flat base type
- Copper base plate (Nickel-plating)
- RoHS Directive compliant
- Tin-plating pin terminals



CM600DX-34T/CM600DXP-34T
HIGH POWER SWITCHING USE
INSULATED TYPE

MAXIMUM RATINGS (T_{vj}=25 °C, unless otherwise specified)
INVERTER PART IGBT/FWD

Symbol	Item	Conditions	Rating	Unit
V_{CES}	Collector-emitter voltage	G-E short-circuited	1700	V
V_{GES}	Gate-emitter voltage	C-E short-circuited	± 20	V
I_C	Collector current	DC, T_C=76 °C (Note2, 4)	600	A
I_{CRM}		Pulse, Repetitive (Note3)	1200	
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MODULE

Symbol	Item	Conditions	Rating	Unit
V_{isol}	Isolation voltage	Terminals to base plate, RMS, f=60 Hz, AC 1 min	4000	V
T_{vjmax}	Maximum junction temperature	Instantaneous event (overload) (Note10)	175	°C
T_{Cmax}	Maximum case temperature	(Note4, 10)	125	
T_{vjop}	Operating junction temperature	Continuous operation (under switching) (Note10)	-40 ~ +150	°C
T_{stg}	Storage temperature	-	-40 ~ +125	

Figure 15 MITSUBISHI CM600DX-34T datasheet

3.2. CONTROL SECTION

The control system is based on CompactRIO (cRIO) architecture made by National Instruments. The model selected for this project is the *cRIO 9036*, a high-performance control system with several industrial I/O modules, extreme ruggedness, and compliance with the majority of industry-standard certifications.

In general, the control system is divided into two main parts:

1. *Fast Controller* - managing the control loops and the interfacing with the external control network;
2. *Slow Controller* - monitoring the status of the whole system.

Fast controller and slow controller are included in the same system and connected by an Ethernet communication.

In the following paragraphs, the main parts of software and control electronics are presented:

- Fast Controller
- Current sensors & voltage transducers
- Slow control
- Interface with Personnel Protection Interlock System
- Local/Remote Operation
- Operator Interface

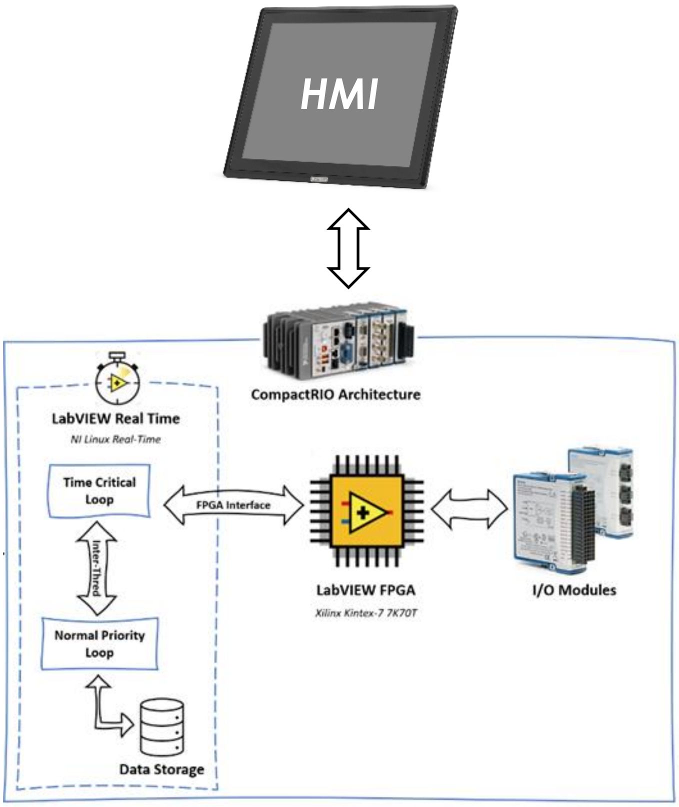

Figure 16 CompactRIO architecture

The architecture of the cRIO is shown in Figure 16~~Figure 16~~. The main software used is LabVIEW, which allows for real-time deployment and distribution of user interface applications for monitoring and controlling the entire system. The cRIO is the Fast Controller of the system, and basically based on two separate units: one for real-time tasks; and the other is the FPGA module for smaller tasks that require high-speed logic and precise timing.

Controller CompactRIO cRIO-9036, 1,33 GHz dual core, 8 slot, FPGA Kintex-7 70T, da -40 °C a 70 °C.

The components of control system are indicated below in the next list.

Controller cRIO 9036: It is real-time controller with high-performance.

CPU	*Intel Atom E3825*
Cores	*2*
CPU frequency	*1.33 GHz*
OS	*NI Linux Real-Time (64-bit)*
Ethernet Ports	*2*
RS-232	*1*
RS-485	*1*
USB	*1 Standard B and 2 Standard A*
SSD	*4 GB*
FPGA	*Xilinx Kintex-7 7K70T*

- **Chassis x8**: The chassis contains the FPGA, and each I/O module is connected directly rather than through a bus; this architecture allows for no control latency for system response.
- **I/O Modules**: Several modules have been chosen to fulfil the MEST control requirements; the details are listed below.

1x **NI 9201 with Screw Terminals**

Voltage range	*+/-10 V*
Sampling rate freq.	*500 kS/s*
Resolution	*12-Bit*
Terminal type	*8-Ch AI Module*

1x **NI-9210 C Series Temperature Input Module**

Number of channels	*4 thermocouple channels*
Sampling rate freq.	*14 S/s/ch*
Resolution	*24-Bit*
Terminal type	*Thermocouple C Series*

1x **NI 9375 with Spring Terminals**

Number of Inputs	*16-Ch sinking DI*
Number of Outputs	*16-Ch sourcing DO*
Voltage range	*0 V to 30 V*
Terminal Type	*Screw*

1x **NI-9862 C Series CAN Interface Module**

Transceiver	*NXP TJA1041AT*
Max baud rate	*1 Mbps*
CAN_H, CAN_L bus lines voltage	*-27 to +40 VDC*
CAN Supply voltage range (V_{SUP})	*+9 to +30 VDC*

1x **IRS Optical Interface 2-fold Tx/Rx 10 Mbit/s**

Fibre Connection	*Versatile Link*
Data rate	*10 Mbit/s typ.*
Transmitters	*3*
Receivers	*3*

1x **TSM-1012 Touch Screen Monitor**

LCD Display	*305 mm (12 in.) (4:3)*
Maximum Resolution	*1024 × 768*
Brightness (cd/m^2)	*600*
Contrast Ratio	*700:1*
LCD Color	*16.2 M*
Pixel Pitch	*0.24 mm × 0.24 mm*
Viewing Angle (H-V)	*160°/140°*
Backlight MTBF	*50,000 hours*

3.3. SUPERCAP MODULES

For the supercapacitors choice, several offers from different suppliers have been taken into account, the main offers are reported on the following table.

The following table summarises the received offers, they compared under four different aspects (namely: Technical solution, Control interface, Lead time estimated, Price), and rated for each of the four fields with a mark ranging from 0 to 10 (the higher the better).

In the last column there is the total score that each offer received, the highest score corresponds to the preferred solution.

Supplier	Hardware solution	Control interface	Lead Time Estimatied	Price	TOTAL
CapTop	8	8	9	10	**35**
Eaton	8	5	7	8	**28**
Skeleton	8	9	9	4	**30**

From the hardware point of view the solutions are equivalent among each other, all the suppliers propose a connection of two parallel and 8 or 16 series (depending on the voltage rating of the specific module). In all the cases, the capacity EOL of the storage bank would be safely above the value of 12,7F considered during simulations.